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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/847,922	05/03/2001	Sameer V. Ovalekar	Ovalekar 4	6553

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MENDELSOHN AND ASSOCIATES PC
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EXAMINER	
PERILLA, JASON M	

ART UNIT	PAPER NUMBER
2634	

DATE MAILED: 09/03/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/847,922	OVALEKAR, SAMEER V.	
	Examiner	Art Unit	
	Jason M Perilla	2634	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 May 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *03 May 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-15 are pending in the instant application.

Specification

2. Applicant is reminded of the proper language and format for an abstract of the disclosure.

The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet **within the range of 50 to 150 words**. It is important that the abstract not exceed 150 words in length since the space provided for the abstract on the computer tape used by the printer is limited. The form and legal phraseology often used in patent claims, such as "means" and "said," should be avoided. The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details.

The language should be clear and concise and should not repeat information given in the title. It should avoid using phrases which can be implied, such as, "The disclosure concerns," "The disclosure defined by this invention," "The disclosure describes," etc.

Claim Objections

3. Claims 3 and 5 are objected to because of the following informalities:

Regarding claim 3, the phrase, "wherein each add/subtract logic unit" in line 1 should be replaced by --wherein for each add/subtract logic unit— for clarity of the claim language.

Regarding claim 5, the variable M should be defined in the claim to be of integer type.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Levison et al (US 6366938; hereafter "Levison") in view of Lee (US 5822365).

Regarding claim 1, Levison discloses an apparatus for correlating a sequence of received samples with chip values of a locally generated sequence by figure 2, the apparatus comprising: a first set of combiners (24 and leftmost column of adder tree 25) configured as a first level of a tree structure to receive the sequence of received samples in groups (i.e. the output of sign inverters having spreading code inputs C7 and C8 comprise 1 group), each combining a group of at least two samples based on corresponding chip values (C7 and C8) of the locally generated sequence to generate a correlation value for the group at the first level; and a second set of combiners (remaining columns of adder tree 25) configured as one or more additional levels of the tree structure, wherein, each combiner of the second set combines a group of at least two correlation values of a previous level of the tree structure to generate a correlation value for the group at a current level of the tree structure (col. 4, lines 39-63). Levison discloses the correlation apparatus but does not specifically disclose how it may be applied in the case of the reception of a signal having one of a plurality of spreading rates or various chip rates. Hence, Levison does not clearly disclose that each combiner of the first and second sets comprises an output tap that enables the corresponding correlation value to be read out of the tree structure for one of the plurality of spreading rates. However, it is clearly apparent that the tree structure could

be generated for any one of a plurality of chip lengths. Levison discloses the structure of the tree correlator and how it would be generated in the case of a length M chip code (i.e. a variable chip code length; col. 3, lines 10-45). Thereby, Levison discloses that the number of adder tree levels directly depends on the number of chips in the spreading code. Further, Lee discloses a variable spreading code length correlator and teaches that a variable length correlator has the advantage that it does not need to be reconfigured or replaced in the case of a variable spreading code length (col. 1, lines 52-60; col. 2, lines 50-55; col. 4, lines 45-53). Therefore, it would have been obvious to one having ordinary skill in the art at the time which the invention was made to provide output taps on the tree structure of Levison to enable the corresponding correlation value to be read out of the tree structure for any one of a plurality of spreading rates because, as taught by Lee, the correlation circuit would not need to be replaced or modified because of a change in the length of the spreading code sequence.

Regarding claim 2, Levison in view of Lee disclose the limitations of claim 1 as applied above. Further, Levison discloses that each of the first set of combiners is an add/subtract logic unit (fig. 2, ref. 24; col. 4, lines 40-50). The first set of combiners is comprised of the sign-changers (24) which define the sign of the incoming received chip code according to the reference chip code (Cn-C9) as well as sum circuits (leftmost first column of adder tree 25).

Regarding claim 3, Levison in view of Lee disclose the limitations of claim 2 as applied above. Further, Levison discloses that each add/subtract logic unit the chip

values dictate whether the corresponding samples are inverted prior to combining by the sign-changers (fig. 2, ref. 24; col. 4, lines 40-50).

Regarding claim 4, Levison in view of Lee disclose the limitations of claim 1 as applied above. Further, Levison discloses that each of the second set of combiners is an adder. Each of the second set of combiners comprises a column of the adder tree (fig. 2, ref. 25) excluding the first leftmost column which is part of the first set of combiners.

Regarding claim 5, Levison in view of Lee disclose the limitations of claim 1 as applied above. Further, Levison discloses that the plurality of spreading rates includes a maximum spreading rate N that is of length X^M, where X is a positive integer, and each other of the plurality of spreading rates is less than the maximum spreading rate N and is of length X^m, $1 \leq m \leq M$. It is inherent that in the system of Levison in view of Lee that there would be a maximum spreading rate or spreading chip code length defined by the number of registers (fig. 2, ref. 23). No extra registers could be added in the case of a spreading code chip length of greater than N which is equal to the number of registers, and therefore, the maximum length is N. Further, in the system of Levison in view of Lee according to figure 2 of Levison, the value of X is 2 because the adders in the adder tree sum two chips and the value of M is 4 because N (the number of registers 23) is 16 ($2^4=16$). Therefore, it follows that any of the plurality of spreading chip code lengths less than the maximum N (16 according to figure 2) would be defined as having length X^m where $1 \leq m \leq M$ because each of the summing circuits in the adder

tree add two chips and m could never be greater than M because there could never be more than X^M=N registers without a change in the design of the circuit.

Regarding claim 6, Levison in view of Lee disclose the limitations of claim 5 as applied above. Further, Levison discloses by figure 2 that each of the first set of combiners is an add/subtract logic unit that combines X input samples based on X chip values of the locally generated sequence, and each of the second set of combiners is an adder, each adder receiving X correlation values for a group from the previous level.

Regarding claim 7, Levison in view of Lee disclose the limitations of claim 5 as applied above. Further, Levison discloses that X=2 as applied in claim 5 above.

Regarding claim 8, Levison in view of Lee disclose the limitations of claim 1 above. Further, figure 2 of Levison is embodied as a circuit.

Regarding claim 9, Levison in view of Lee disclose the limitations of claim 8 as applied above. Further, it would have been obvious to one having ordinary skill in the art to implement the circuit of figure 2 of Levison as an integrated circuit. Levison discloses the exemplary embodiment of the invention with relation to the size of the circuit of figure 2 corresponding to substrate area of an integrated circuit (col. 8, lines 5-10). Therefore, Levison implies that the exemplary embodiment of the invention would be created as an integrated circuit, and it is obvious that the circuit of figure 2 would likewise be implemented as an integrated circuit because integrated circuits provide the advantages of low power and small size.

Regarding claim 10, Levison in view of Lee disclose the limitations of claim 8 as applied above. Further Levison discloses that the correlator is used in a code-division multiple access (CDMA) system (col. 1, lines 20-25).

Regarding claim 11, Levison in view of Lee disclose the limitations of the method of claim 11 as applied to apparatus of claim 1 above.

Regarding claim 12, Levison in view of Lee disclose the limitations of the claim as applied to claim 5 above.

6. Claims 13-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Levison in view of Lee, and in further view of Davidovici (US 5894494).

Regarding claim 13, Levison in view of Lee disclose the limitations of claim 11 as applied above. Levison does not explicitly disclose that the method is embodied in steps of a processor in an integrated circuit. However, Davidovici discloses a correlator circuit (abstract) which may be embodied as steps of a processor (software; col. 9, lines 23-35). The use of processors is well known in the art and they provide the advantage of being able to carry out a plurality of tasks defined by software. Therefore, it would have been obvious to one having ordinary skill in the art at the time which the invention was made to embody the method of Levison in view of Lee as steps of a processor in an integrated circuit as taught by Davidovici because the methods of the processor could be tailored to include a plurality of steps according to the correlation method and methods of a plurality of other processes easily by the use of software.

Regarding claim 14, Levison in view of Lee disclose the limitations of claim 11 as applied above. Further, Levison discloses that the method is applied in a CDMA system

(col. 1, lines 20-25), and the use of a processor to implement the method is obvious in view of Davidovici as applied to claim 13 above.

Regarding claim 15, Levison in view of Lee disclose the limitations of the method of claim 11 as applied to apparatus of claim 1 above. Levison in view of Lee do not disclose that the method is embodied as computer readable media executable by a processor to perform the steps of the method. However, Davidovici discloses a correlator circuit (abstract) which may be embodied as steps of a processor (software; col. 9, lines 23-35). The use of processors is well known in the art and they provide the advantage of being able to carry out a plurality of tasks defined by software. Therefore, it would have been obvious to one having ordinary skill in the art at the time which the invention was made to embody the method of Levison in view of Lee as software executable by a processor as taught by Davidovici because the methods of the processor could be tailored to include a plurality of steps according to the correlation method and methods of a plurality of other processes easily by the use of the software.

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The following prior art of record not relied upon above is cited to further show the state of the art with respect to variable length correlators.

U.S. Pat. No. 6181733 to Shinde.

U.S. Pat. No. 6005903 to Mandelovicz.

U.S. Pat. No. 6148313 to Freidin et al.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jason M Perilla whose telephone number is (571) 272-3055. The examiner can normally be reached on M-F 8-5 EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Steven Chin can be reached on (571) 272-3056. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jason M. Perilla
August 30, 2004

jmp

CHIEH M. FAN
PRIMARY EXAMINER